METHOD OF FABRICATING CAPACITOR

DESCRIPTION

BACKGROUND OF THE INVENTION

[Para 1] Field of the Invention

[Para 2] The present invention relates to a method of fabricating a semiconductor device. More particularly, the present invention relates to a method of fabricating a capacitor that can improve the quality of the inter-electrode dielectric layer and reduce the electrical resistance of the lower electrode to increase the Q-factor of the capacitor.

[Para 3] Description of the Related Art

[Para 4] In the prior art, a capacitor compatible to MOS process usually has a metal-insulator-metal (MIM) structure or metal-insulator-silicon (MIS) structure. However, a MIM or MIS capacitor suitable to high-voltage applications is usually insufficient in the capacitance per unit area. Meanwhile, for mixed-mode devices or RF devices including capacitors, it is frequently required to save a large area of the die for the capacitors to achieve sufficient capacitance satisfying the design rule. However, after the semiconductor industry advanced to deep sub-micron generation, increasing the capacitor area will reduce the integration degree of devices more significantly so that the economic effect of manufacture is lowered more. Therefore, increasing the unit-area capacitance of the capacitors is always desired in the semiconductor industry.

[Para 5] In view of the foregoing, a capacitor fabricating method integrated with MOS process is proposed. In the method, a doped region is formed in a semiconductor substrate as a lower electrode, and then an oxide layer as the

dielectric layer of the capacitor is grown on the doped region simultaneously with the gate oxide layers in the MOS area on the same die. A polysilicon layer is formed covering the capacitor dielectric layer and the gate oxide layer, and is then patterned into gates and an upper electrode of the capacitor.

[Para 6] Nevertheless, since the dielectric layer is formed after the doping step for forming the lower electrode, the quality thereof is not good. Meanwhile, the dopant concentration in the doped region is not so uniform. Moreover, the lower electrode constituted of a doped region has a higher resistance than metal, so that the Q-factor of the capacitor is usually too small to satisfy high-frequency applications.

SUMMARY OF THE INVENTION

[Para 7] Accordingly, one object of this invention is to provide a method of fabricating a capacitor that can improve the quality of the capacitor dielectric layer.

[Para 8] Another object of this invention is to provide a method of fabricating a capacitor that can lower the resistance of the capacitor to increase the Q-factor of the same.

[Para 9] A method of fabricating a capacitor of this invention includes the following steps. A dielectric layer is formed on a semiconductor substrate, and an upper electrode having multiple openings therein is formed on the dielectric layer. A doping step is then performed to the substrate through the openings to form a single doped region as a lower electrode in the substrate under the upper electrode.

[Para 10] In an embodiment of this invention, the upper electrode is made from doped polysilicon, and a spacer is further formed on the sidewall of each opening in the upper electrode after the lower electrode is formed. Then, a self-aligned silicide (salicide) process is performed to form meal silicide layers on the upper electrode and the exposed portions of the doped region as the lower electrode.

[Para 11] In another embodiment of this invention, the upper electrode is also made from doped polysilicon. However, this embodiment differs from the previously one in that a liner layer is formed on the sidewall of each opening prior to formation of the spacer and the spacer is removed before the salicide process. The spacer is removed to increase the area of the metal silicide layer that will be formed on the lower electrode.

[Para 12] Since the dielectric layer is formed before the doping step, the quality of the dielectric layer under the upper electrode is better. Moreover, by incorporating a salicide process after the lower electrode is formed, the resistance of each of the upper and lower electrodes can be reduced to increase the Q-factor of the capacitor.

[Para 13] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 14] FIGs. 1A and 1B(a)/(b) illustrate a process flow of fabricating a capacitor according to a first embodiment of this invention in a cross-sectional view, wherein two different doping methods for forming the lower electrode are shown in FIG. 1B(a) and FIG. 1B(b), respectively.

[Para 15] FIGs. 2A-2B illustrate a latter part of a process flow of fabricating a capacitor according to a second embodiment of this invention in a cross-sectional view.

[Para 16] FIGs. 3A-3B illustrate a latter part of a process flow of fabricating a capacitor according to a third embodiment of this invention in a cross-sectional view.

[Para 17] FIG. 4 illustrates an example of an upper electrode structure of a capacitor according to the embodiments of this invention in a top view.

[Para 18] FIG. 5 illustrates another example of an upper electrode structure of a capacitor according to the embodiments of this invention in a top view.

[Para 19] FIG. 6 illustrates yet another example of an upper electrode structure of a capacitor according to the embodiments of this invention in a top view.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Para 20] First Embodiment

[Para 21] FIGs. 1A and 1B(a)/(b) illustrate a process flow of fabricating a capacitor according to the first embodiment of this invention in a cross-sectional view, wherein two different doping methods for forming the lower electrode are shown in FIG. 1B(a) and FIG. 1B(b), respectively.

[Para 22] Referring to FIG. 1A, a semiconductor substrate 200 is provided, which may be a single-crystal silicon substrate. A dielectric layer 202 is formed on the substrate 200, preferably together with the gate dielectric layers in the MOS area (not shown) of the same substrate 200. For example, the dielectric layer 202 can be a silicon oxide layer that is formed simultaneously with the gate oxide layers in the MOS area through thermal oxidation.

[Para 23] Then, an upper electrode 204 having multiple openings 205 therein is formed on the dielectric layer 202. The steps for forming the upper electrode 204 may include forming a doped polysilicon layer on the dielectric layer 202 and patterning the same with a lithography process and an etching process, which may also remove the dielectric layer 202 exposed in the openings 205, as shown in FIG. 1B. The upper electrode 204 is preferably formed simultaneously with the gates in the MOS area (not shown). That is, the upper electrode 204 and the gates in the MOS area can be formed from the same conductive layer, such as, a doped polysilicon layer as mentioned in the above example.

[Para 24] In a top view, the upper electrode 204 may include multiple bar-like conductive layers 204a connected to each other with trench-like openings 205 between them. Examples of such an upper electrode structure include a comb-like structure as shown in FIG. 4 and a fishbone-like structure as shown in FIG. 5. Alternatively, the upper electrode 204 may have a net-like structure

as shown in FIG. 6, which has multiple meshes therein as the openings 205. The line IV-IV'/V-V'/ VI-VI' in FIG. 4/5/6 corresponds to the cross-section of FIG. 1A.

[Para 25] Referring to FIG. 1B(a)/(b), a doping step is then performed to the substrate 200 through the openings 205 in the upper electrode 204 to form a doped region 208 as a lower electrode under the upper electrode 204. The doping step can be done with tilt ion implantation 206, as shown in FIG. 1B(a). With the tilt ion implantation 206, a doped region 208a is formed under each opening 205 extending to the substrate 200 under the portions 204a of the upper electrode 204 to connect adjacent doped regions 208a, so that the doped regions 208a merge into a single doped region 208.

[Para 26] Referring to FIG. 1B(b), the doping step may alternatively includes vertical ion implantation 209 for forming multiple doped regions 208a under the openings 205, and an annealing process for diffusing the implanted dopants to make the doped regions 208a merge into a single doped region 208.

[Para 27] Since the dielectric layer 202 is formed before the doping step for forming the lower electrode 208, the quality of the dielectric layer 202 is better than that in the prior art. Moreover, when the dielectric layer 202 formed before the doping step is formed with thermal oxidation, the thickness thereof can be about one half of that of an oxide layer formed with thermal oxidation after the doping step as in the prior art. An oxide layer formed on a heavily doped substrate with thermal oxidation, as in the prior art, is thicker because of the high dopant concentration in the substrate. Accordingly, the capacitance of the capacitor is not reduced even though the area of the upper electrode 204 is reduced due to presence of the openings 205.

[Para 28] Second Embodiment

[Para 29] FIGs. 2A-2B illustrate a latter part of a process flow of fabricating a capacitor according to the second embodiment of this invention in a cross-sectional view. The former part of the process flow is described in the first embodiment, while the step of FIG. 2A is subsequent to the step of FIG. 1B and the same elements are labeled with the same reference numbers.

[Para 30] Referring to FIG. 2A, a spacer 210 is formed on the sidewall of each opening 205 in the upper electrode 204. The spacers 210 may be formed simultaneously with the spacers on the sidewalls of the gates in a MOS area (not shown) on the same substrate 200. The spacers 210 are formed by, for example, forming a conformal insulating layer (not shown) over the substrate 200 and then anisotropically etching the same to remove portions thereof. The material of the insulating layer may be silicon nitride, and the method for forming the same is chemical vapor deposition (CVD), for example.

[Para 31] Referring to FIG. 2B, a self-aligned silicide (salicide) is conducted to form metal silicide layers 212 and 212a on the top of the upper electrode 204 and the exposed surfaces of the doped region 208, respectively. The material of the metal silicide layer 212/212a can be a silicide of a refractory metal, wherein the refractory metal is selected from the group consisting of Ti, W, Pt, Co and Ni. In a salicide process forming titanium silicide, for example, a titanium layer of about 300Å in thickness is formed over the substrate 200 with sputtering. Then, a rapid thermal process is conducted under 700° for 20 seconds to react the titanium layer with underlying silicon atoms of the upper electrode 204 and the substrate 200 to form titanium silicide layers thereon. The unreacted titanium metal is then removed using selective wet etching.

[Para 32] Since metal silicide layers 212/212a are formed on the upper electrode 204 and the exposed surfaces of the doped region 208 as the lower electrode, the bulk resistance and contact resistance of the upper and lower electrodes can be reduced to increase the Q-factor of the capacitor.

[Para 33] Third Embodiment

[Para 34] FIGs. 3A-3B illustrate a latter part of a process flow of fabricating a capacitor according to the third embodiment of this invention in a cross-sectional view. The former part of the process flow is described in the first embodiment, while the step of FIG. 3A is subsequent to the step of FIG. 1B and the same elements are labeled with the same reference numbers.

[Para 35] Referring to FIG. 3A, after the lower electrode 208 is formed, a liner layer 214 is formed on the sidewall of each opening 205 in the upper electrode 204, and then a spacer 210 is formed on each liner layer 214. The liner layer

214 may include silicon oxide and may be formed with thermal oxidation, for example. The forming method and the material of the spacer 210 may be the same as those in the second embodiment.

[Para 36] Referring to FIG. 3B, the spacers 210 are removed with, for example, isotropic etching, leaving the liner layers 214 on the sidewalls of the openings 205. It is particularly noted that the liner layers 214 and the spacers 210 are formed sequentially in a MOS process designed for the MOS area on the same substrate 200, while the spacers 210 are removed to increase the exposed area of the lower electrode 208. When the MOS process does not form spacers, the step of forming spacers on sidewalls of the openings 205 and the step of removing spacers surely can be saved.

[Para 37] Referring to FIG. 3B again, a salicide process is conducted to form metal silicide layers 212 and 212b on the top of the upper electrode 204 and the exposed surfaces of the doped region 208, respectively. The material of the metal silicide layer 212/212a can be a silicide of a refractory metal, wherein the refractory metal is selected from the group consisting of Ti, W, Pt, Co and Ni.

[Para 38] Since metal silicide layers 212/212b are formed on the upper electrode 204 and the exposed surfaces of the doped region 208 as the lower electrode, the bulk resistance and the contact resistance of the upper and lower electrodes can be reduced to increase the Q-factor of the capacitor. In addition, the bulk resistance and the contact resistance of the lower electrode 208 is even lower than those of the lower electrode in the second embodiment, since the spacers 210 are removed to increase the exposed area of the lower electrode 208.

[Para 39] In summary, since the dielectric layer is formed before the doping step, the quality of the dielectric layer is better than that in the prior art. Moreover, since metal silicide layers are formed on the upper electrode and the exposed surfaces of the doped region as the lower electrode, the bulk resistance and the contact resistance of the upper and lower electrodes can be reduced to increase the Q-factor of the capacitor.

[Para 40] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.